threshold signal adapts to the level of the input signal in the low-ohmic state of the resistor (22).

5. A circuit arrangement as claimed in claim 1, characterized in that the threshold value circuit (30) is constituted by a comparator whose first input (32) is positive and whose second input (34) is negative.

6. A circuit arrangement as claimed in claim 1, characterized in that the detector circuit (40) comprises at least a slope detector unit (42) and at least a clock regaining unit (44) connected to the slope detector unit (42), and in that the detector circuit (40) regenerates the data clock (f_{data}) from the digital output signal.

8. A circuit arrangement as claimed in claim 1, characterized in that the control circuit (50) has an externally and/or internally triggerable reset function.

10. A circuit arrangement as claimed in claim 8, characterized in that, after triggering the reset function of the control circuit (50), the capacitive element (24) is chargeable to a given capacitance (C_t).